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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/659,872	09/13/2000	Hartmund Terletzki	00P7882US	7001

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EXAMINER
NGUYEN, MINH T

ART UNIT	PAPER NUMBER
2816	16

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/659,872	TERLETZKI ET AL.	
	Examin r	Art Unit	
	Minh Nguyen	2816	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6* is/are allowed.

6)☒ Claim(s) *1,9 and 15-30* is/are rejected.

7)☒ Claim(s) *2-8 and 10-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 April 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Applicants' appeal brief and amendment filed on 11/18/02 have been received and entered in the case. In view of the current consideration, new grounds of rejections are needed as set forth below. This action is NON-FINAL.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 9 and 15-30 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,748,024, issued to Takahashi et al (a copy of the reference was provided in paper number 8).

As per claim 1, Takahashi discloses a level shifting circuitry (Fig. 4), comprising:

a level-shifting section (transistor 22 and 23) responsive to an input logic signal 31, such input logic signal having a first voltage level representative of a first logic state or a second voltage level representative of a second logic state (Fig. 5), such level-shifting section providing an output logic signal OUTPUT at an output terminal 33 thereof having a third voltage level representative of the first logic state of the input logic signal; and a fourth voltage level representative of the second logic state of the input signal (Fig. 5);

an enable/disable section (transistors 21 and 24) coupled to the level shifting section, the enable/disable section being responsive to an enable/disable signal 32, the enable/disable section placing the output terminal at a relatively high output impedance condition independent of the logic state of the input logic signal during a disable mode (Fig. 5).

As per claim 9, Takahashi discloses a level shifting circuit (Fig. 4), comprising:

an input node 31 to receive an input signal, the input signal varying between a first voltage level and a second voltage level (see Fig. 5);

a first n-channel transistor 23 having a first source/drain region, a second source/drain region and a gate, the gate being coupled to the input node 31;

a second n-channel transistor 24 having a first source/drain region coupled to the second source/drain region of the first n-channel transistor, a second source/drain region coupled to a second voltage level reference node VSS and a gate coupled to a first enable signal node 32;

a first p-channel transistor 22 having a first source/drain region coupled to the first source/drain region of the first n-channel transistor, a second source/drain region and a gate coupled to the input node 31;

a second p-channel transistor 21 having a first source/drain region coupled to the second source/drain region of the first p-charnel transistor, a second source/drain region coupled to a third reference node VDD and a gate coupled to a second enable signal node (the output terminal node of the inverter 13), the third reference node carrying a third voltage level, the third voltage level being different than the first voltage level (Fig. 5).

As per claim 15, Takahashi further discloses a signal carried at the first enable signal node is an inverted version of a signal carried at the second enable signal node (by the inverter 13).

As per claim 16, Takahashi further discloses an inverter 13 coupled between the first enable signal node and the second enable signal node, the inverter including a level shifting circuit (the inverter 11).

As per claim 17, Takahashi further discloses the inverter 13 includes an input coupled to the first enable signal node 32 and an output coupled to the second enable signal node (at the gate of transistor 21).

As per claim 18, Takahashi further discloses the third voltage level is greater than the first voltage level (because VDD must be larger than the input voltage).

As per claim 19, since Takahashi circuit can function when the third voltage level is 2.5 volts and the first voltage level is 2.1 volts, the recited limitation is met.

As per claim 20, Takahashi discloses a level shifting circuit (Fig. 4) comprising:

a level-shifting section (transistors 22 and 23) responsive to an input logic signal 31, the input logic signal varying between a first voltage level LOW and a second voltage level HI, the level-shifting section providing an output logic signal OUTPUT at an output terminal 33 thereof, the output logic signal varying between the first voltage level LOW and a third voltage level (VDD less the voltage drop across transistors 21 and 22), the third voltage level being different than the second voltage level (because VIN high is not the same as VDD less the voltage drop across transistors 21 and 22);

a first reference voltage node VSS carrying a voltage at the first voltage level LOW;

a third reference voltage node VDD carrying a voltage at the third voltage level VDD; and

an enable/disable section (transistors 24 and 21) including a first portion (transistor 24 coupled between the level shifting section and the first reference voltage node VSS and a second portion (transistor 21) coupled between the level shifting section and the third reference voltage node VDD, the enable/disable section being responsive to an enable/disable signal 32, the enable/disable section causing the output terminal to be placed. at a relatively high output impedance condition independent of the logic state of the input logic signal in response to a disable mode indication from the enable/disable signal (see Fig. 5).

As per claim 21, Takahashi further discloses the first voltage level LOW and the third voltage levels VSS are representative of a first logic state and wherein the second voltage level HI is representative of a second logic state.

As per claim 22, Takahashi further discloses the level-shifting section comprises:

a first transistor 22 with a current path coupled between the third reference voltage node VDD and the output terminal 33; and

a second transistor 23 with a current path coupled between the output terminal 33 and the first reference voltage node VSS.

As per claim 23, Takahashi further discloses the enable/disable section comprises:

a third transistor 21 with a current path coupled in series the current path of the first transistor 22, the current path of the third transistor 21 coupled between the third reference voltage node VDD and the first transistor; and

a fourth transistor 24 with a current path coupled in series the current path of the second transistor 23, the current path of the fourth transistor 24 coupled between the first reference voltage node VSS and the second transistor.

As per claim 24, Takahashi further discloses both the third and fourth transistors are rendered conductive when the enable/disable signal indicates that the level shifting circuit is in an enable mode and wherein both the third and fourth transistors are rendered non-conductive when the enable/disable signal indicates that the level shifting circuit is in the disable mode (see Fig, 5).

As per claim 25, Takahashi discloses the first portion of the enable/disable section comprises a first switch (transistor 24) between the level shifting section and the first reference voltage node VSS and wherein the second portion of the enable/disable section includes a second switch (transistor 21) coupled between the level shifting second and the third reference voltage node VDD.

As per claim 26, Takahashi further discloses an inverter 13 coupled between a control terminal of the first switch and a control terminal of the second switch.

As per claim 27, Takahashi further discloses the inverter 13 includes an input coupled to the control terminal of the first switch and an output coupled to the control terminal of the second switch (as shown).

As per claim 28, since all the elements in the Takahashi are connected, the inverter 13 is coupled to the third reference voltage node.

As per claim 29, Takahashi further discloses the inverter 13 includes a level shifter (the inverter 11 coupled to the third reference voltage node VSS and to a voltage node at the first voltage level.

As per claim 30, Takahashi further discloses the first and second switches comprise MOS transistors (as shown).

Response to Arguments

3. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Allowable Subject Matter

4. Claims 2-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 2-8 are allowable because the prior art of record fails to disclose or suggest a level shifter circuit which includes an input transistors connected as recited in claim 2.

Claims 10-14 are allowable for the same reason noted in claim 2 as recited in claim 10.

5. Claim 6 is allowed for the reason noted in the previous Office Action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is 703-306-9179. The examiner can normally be reached on Monday - Thursday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Minh Nguyen
Examiner
Art Unit 2816

MN
February 8, 2003